REMARKS

Claims 1-24 remain pending in the application. Claims 1, 3, 12-13, 15-16, and 20-23 have been amended.

Claims 3-12-13 and 20-23 stand objected to under 37 C.F.R. 1.75 (c) as being of improper dependent form for failing to further limit the subject matter of a previous claim.

In response, Applicants have now amended the above identified claims to remove the stated objections.

In view of the foregoing, Applicants believe that they have now removed the stated objections to grounds Claims 3-12-13 and 20-23 based on 37 C.F.R. 1.75 (c)

Claims 1-5, 12-18, 20-24 stand rejected under 35 U.S.C. 102(b) as being anticipated by Saito et al. (U.S. Patent No. 6,320,800) (Saito).

Applicants have now amended claim 1 to further distinguish their invention from Saito's. Applicants submit that Saito teaches how to "replace" a defective element by using an "address comparison means (i.e., 313in Fig. 4C) in an architecture that includes a multi-bank operation. In contradistinction, Applicants teach how to detect the presence of a defective element in the memory using "allocation means" in which a defective element is identified. Such a defective address is found by way of "data comparison means" as recited in amended Claim 1.

Applicants respectfully point out that the Office Action last paragraph in page 3 states the following:

"With regard to claim 1, Saito discloses a memory device configured to perform multi-bank operations comprising: a plurality of memory banks (fig. 3, Bank, Bank0) including at least a first (fig.3, Bank 0) and second (fig. 3, Bank1) memory bank respectively controlled by a first (fig 3, 304 of Bank0) and second (fig. 3, 304 or bank1) redundancy replacement means , and means (fig. 4A, 313a or bank1) redundancy replacement means, and means (fig. 4A, 313a) for comparing **data bits read out from said first memory bank**" [emphasis is Applicant's]

Applicants respectfully point out that 313 is an Address Comparator and therefore is not intended to compare data bits). Applicants further state that Saito's fig. 4A shows the input of 313a coupled to address buffer 307. It, therefore, cannot be read from the memory cell array 101 which is equivalent to the Applicant's bank as shown in Fig 3.

Continuing in the last paragraph in page 3 of the Office Action, it is further stated:

..... "(fig. 4A, assuming Bank0 is selected for reading) against corresponding **expected data (fig. 4A, from 312)"** [emphasis is Applicant's].

Applicants respectfully traverse this assertion since no expected data is shown nor suggested by Saito in his (Fig. 4a, 312). Applicants contend that 312 in Fig. 4a is a defective address string circuit, and therefore, it does not and cannot provide the expected data to detect if the data bit read from the memory array is the same as the expected data

In summary, Saito teaches means for "replacing" a defective element which is achieved by way of an "address comparison means (i.e., 313 in Fig. 4C) in an architecture that includes a multi-bank operation. Saito's "address comparison means", as the phrase indicates, is limited to handling only addresses. In contradistinction, Applicants teach how to detect the presence of a defective element in the memory using "allocation means" by comparing data bits read out from the memory bank and compared against expected data. Such a defective element is identified by way of a "data comparison means.

Thus, Applicants believe that all the rejected claims are free of rejection under 35 U.S.C. 102(b) over Saito, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

In view of the foregoing amendments and arguments, Applicants respectfully request that all the rejections and objections to this application be reconsidered and withdrawn and that the Examiner pass all the pending claims to issue.

Should the Examiner have any suggestions pertinent to the allowance of this application, the Examiner is encouraged to contact Applicants' undersigned representative.

Respectfully submitted,
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